

PATENT ABSTRACTS OF JAPAN

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(21)Application number : 09-022564 (71)Applicant : SONY CORP
(22)Date of filing : 05. 02. 1997 (72)Inventor : YANAGIDA TOSHIHARU

(54) PRODUCTION OF BUMP

(57)Abstract:

PROBLEM TO BE SOLVED: To provide a method for producing a bump exhibiting high reliability and durability after flip-chip mounting in which contact resistance is decreased by cleaning the surface of a finished bump.

SOLUTION: After ball bumps 8 are formed through a specified process a semiconductor substrate 1 is subjected to sputter etching in Ar gas atmosphere in order to remove an impurity layer 9 from the surface of the ball bump 8 thus exposing the clean surface thereof. Uppermost surface of polyimide 3 is then activated by ion impact. Sputter etching may be carried out in an atmosphere containing a reducing gas. Alternatively the semiconductor substrate 1 may be subjected to ashing in an atmosphere containing oxygen after forming the ball bumps 8 and then subjected to sputter etching in an inert atmosphere or an atmosphere containing at least a reducing gas.

CLAIMS

[Claim(s)]

[Claim 1] A bump manufacturing method having the process of performing sputter etching processing in an inert gas atmosphere to a base after bump formation.

[Claim 2] The bump manufacturing method according to claim 1 wherein the

above-mentioned vamp is a solder ball bump.

[Claim 3]The vamp manufacturing method according to claim 1 performing the above-mentioned sputter etching processing controlling independently a plasma discharge output and bias voltage to the above-mentioned base at least.

[Claim 4]The vamp manufacturing method according to claim 1 more than $1 \times 10^{11} \text{cm}^{-3}$ performing the above-mentioned sputter etching processing with plasma density of less than $1 \times 10^{14} \text{cm}^{-3}$.

[Claim 5]A vamp manufacturing method having the process of performing sputter etching processing in atmosphere which contains reducing gas at least to a base after bump formation.

[Claim 6]The vamp manufacturing method according to claim 5 wherein the above-mentioned vamp is a solder ball bump.

[Claim 7]The vamp manufacturing method according to claim 5 performing the above-mentioned sputter etching processing controlling independently a plasma discharge output and bias voltage to the above-mentioned base at least.

[Claim 8]The vamp manufacturing method according to claim 5 more than $1 \times 10^{11} \text{cm}^{-3}$ performing the above-mentioned sputter etching processing with plasma density of less than $1 \times 10^{14} \text{cm}^{-3}$.

[Claim 9]A vamp manufacturing method having the process of performing sputter etching processing continuously in an inert gas atmosphere or atmosphere which contains reducing gas at least after performing ashing treatment to a base after bump formation in atmosphere which contains oxygen at least.

[Claim 10]The vamp manufacturing method according to claim 9 wherein the above-mentioned vamp is a solder ball bump.

[Claim 11]The vamp manufacturing method according to claim 9 performing the above-mentioned ASSHINNGU processing and/or the above-mentioned sputter etching processing controlling independently a plasma discharge output and bias voltage to the above-mentioned base at least.

[Claim 12]The vamp manufacturing method according to claim 9 more than $1 \times 10^{11} \text{cm}^{-3}$ performing the above-mentioned ashing treatment and/or the above-mentioned sputter etching processing with plasma density of less than $1 \times 10^{14} \text{cm}^{-3}$.

DETAILED DESCRIPTION

[Detailed Description of the Invention]

[0001]

[Field of the Invention] Especially this invention avoids poor generating resulting from residue contamination etc. in a wet back process about a vapor manufacturing method and relates to the vapor manufacturing method for realizing improvement in adhesion with the contact resistance of a vapor surface-protection film and sealing resin.

[0002]

[Description of the Prior Art] In order to develop the miniaturization of electronic equipment further it is an important point how component-mounting density is raised. Things -- development of high-density-assembly arts such as a flip-chip-mounting method which mounts a bare chip to an immediate printing wiring board is briskly performed as substitution of the conventional package mounting also about mounting of an integrated circuit (IC) and large scale integration circuit (LSI).

[0003] One of the PURIPPU chip mounting method of this has a method of mounting the thing in which the solder ball bump was formed on the aluminum (aluminum) electrode pad of an IC chip or an LSI chip in a printed-circuit board. Although there is a method using the electrolytic plating method as a method of forming this solder ball bump on a predetermined Al electrode pad in this case in order that the thickness of the solder film formed may receive the influence by dispersion with slight surface state of a ground and electrical resistance it is fundamentally difficult for height to form the uniformly equal solder ball bump within an IC chip.

[0004] Then the method of forming a solder ball bump from before as a method of controlling dispersion in the height of a solder ball bump using membrane formation of the solder film by a vacuum deposition method and the lift off of a resist pattern is known. An example of the formation process of the solder ball bump by this method is explained below referring to drawing 6.

[0005] Namely in the manufacturing method of this conventional solder ball bump first as shown in drawing 6 a sputtering process and the dry etching method are used for the prescribed position on the semiconductor base substances 101 such as a silicon (Si) wafer in which the circuit element etc. were formed and Al electrode pad 102 of specified shape is formed in it. Next an opening is formed in the portion corresponding to the Al electrode pad 102 top of this passivation film after forming a passivation film (not shown) like a silicon nitride (SiN) film all over the semiconductor base substance 101 for example. Next an opening is formed in the portion corresponding to the Al electrode pad 102 top of this polyimide film 103 after forming a polyimide film on this passivation film for example.

[0006]Nextafter laminating a chromium (Cr) film a copper (Cu) film and a golden (Au) film on the whole surface one by one for example and forming Cr/Cu/Au membrane in it by sputtering process The BLM (Barrier Limiting Metal) film 104 which consists of this patterned Cr/Cu/Au membrane is formed by patterning mostly this Cr/Cu/Au membrane after Al electrode pad 102 and identical shape. This BLM film 104 also has a role of a barrier metal of the solder ball bump formed behind.

[0007]Nextas shown in drawing 6 B After forming a resist film the whole surface on the semiconductor base substance 101 this resist film is patterned after specified shape by the lithography method. The numerals 105 show the resist pattern of the specified shape formed of this. This resist pattern 105 has the opening 106 of a predetermined size into the portion corresponding to the BLM film 104 to therefore the portion corresponding to the Al electrode pad 102 top.

[0008]Nextas shown in drawing 6 C After forming the solder film 107 in the whole surface with a vacuum deposition method as shown in drawing 6 D the resist film 105 is removed with the solder film 107 on it by the lift-off method. Thereby the garbage of the solder film 107 is removed and the solder film 107 is patterned after desired shape. Then by heat-treating and carrying out melting of the solder film 107 as eventually shown in drawing 6 E the almost spherical solder ball bump 108 is formed.

[0009]Here the process of rounding off the solder film 107 spherically by heat treatment shown in drawing 6 E is usually called a wetback.

Supposing the natural oxidation film is thickly formed in the surface of the solder film 107 even if it will heat-treat melting of solder will not progress uniformly but it will become impossible to form the solder ball bump 108 well in this wetback's process.

[0010]Therefore after usually patterning the solder film 107 by a lift off flux which has a reducing action and a surface activity operation beforehand all over the semiconductor base substance 101 before performing a wetback process (the main ingredients) By coating uniformly resinous principle such as an amine system active agent an alcohol solvent rosin and the PORIGURI goal and performing heat treatment from the state. Formation of the solder ball bump 108 promoted and stabilized [that solder is spherically round with melting and surface tension of solder and] is realized.

[0011]

[Problem(s) to be Solved by the Invention] Although organic chemical washing is performed in the manufacturing method of the above-mentioned conventional solder ball bump to the semiconductor base substance 101 (refer to drawing 6 E) after the solder ball bump 108 was formed by heat

treatment and flux is washed out. If the organic component in flux carbonized during heat treatment and it has stuck to the wafer surface at this time or the cleaning method of flux is unsuitable, it may remain in the surface of the solder ball bump 108 or its neighborhood as residue without the ability to remove even after the solid content in flux washing. If the storage state after formation of the solder ball bump 108 is unsuitable and oxidation of the solder ball bump 108 progresses, a natural oxidation film may be formed in the surface. The numerals 109 show impurity films such as a contaminant which adhered in the wetback process and a natural oxidation film of the surface of the solder ball bump 108 among drawing 6. E. Here, the impurity layer 109 of the surface of the expedient top of expression and the solder ball bump 108 was exaggerated and the twist is also actually written thickly.

[0012] Thus, if the impurity layer 109 exists in the surface of the solder ball bump 108 as shown in drawing 7, when applying the probe 110 to the surface of the solder ball bump 108 and measuring an electrical property, and the impurity layer 109 intervenes among both contact resistance becomes large and will cause the fault of it becoming impossible to perform exact evaluation etc. In such the state when flip chip mounting is carried out, contact resistance with a printed-circuit board will also increase.

[0013] Although **** is a problem in case the impurity layer 109 exists in the surface of the solder ball bump 108, the residue thing resulting from a process contamination etc. will remain actually also on the polyimide film 103 which is the outermost surface of the chip in which the solder ball bump 108 was formed. When flip chip mounting of the chip of this state is carried out on a printed-circuit board, the adhesion strength between the polyimide film 103 and sealing resin becomes weak and originates in it. It leads also to a crack occurring in the solder ball bump 108 and bonding strength deteriorating or causing the fall of a reliability life by the rise of connection resistance.

[0014] Therefore, there is the purpose of this invention in providing the vapor manufacturing method which has high reliability and endurance after flip chip mounting while it defecates the surface of the vapor after a result and aims at reduction of contact resistance.

[0015]

[Means for Solving the Problem] To achieve the above objects, a vapor manufacturing method by the 1st invention in this invention has the process of performing sputter etching processing which used inactive gas after bump formation.

[0016] A vapor manufacturing method by the 2nd invention in this invention

has the process of performing sputter etching processing after bump formation in atmosphere which contains reducing gas at least.

[0017] A bump manufacturing method by invention of the 3rd of this invention has the process of performing sputter etching processing continuously in inactive gas or atmosphere which contains reducing gas at least after performing ashing treatment after bump formation in atmosphere which contains oxygen at least.

[0018] In a typical embodiment of this invention a bump is a solder ball bump.

[0019] Sputter etching processing is performed in a suitable embodiment of this invention controlling independently a plasma discharge output and bias voltage to a base. A plasma treatment apparatus which has two independently controllable RF generators is used for sputter etching processing in this case in a plasma discharge output and bias voltage at least.

[0020] In other suitable embodiments of this invention more than $1 \times 10^{11} \text{ cm}^{-3}$ performs sputter etching processing with plasma density of less than $1 \times 10^{14} \text{ cm}^{-3}$. In sputter etching processing in this case a source of ICP (Inductively Coupled Plasma) A plasma treatment apparatus which has sources of high density plasmas such as a source of TCP (Transfer Coupled Plasma) an ECR (Electron Cyclotron Resonance) plasma source or a source of helicon wave plasma is used.

[0021] Since it has the process of performing sputter etching processing in inert gas atmosphere such as Ar gas to a base after bump formation according to the 1st invention by this invention constituted as mentioned above The surface of a pure bump can be exposed by removing a natural oxidation film and process residue which were formed on the surface of a bump. By this contact resistance with a probe at the time of measuring electrical resistance and contact resistance with a printed-circuit board after flip chip mounting can be reduced by the surface of a bump after a result being defecated. While the electrical property of a device which produced a bump is improved as for these results reliability and endurance of a product assembled by carrying out flip chip mounting of this device can be substantially raised compared with the former.

[0022] According to the 2nd invention in this invention a bump which has higher reliability than the 1st invention can be formed. Like a case of the 1st invention although sputter etching processing is performed to a base after bump formation specifically sputter etching processing is performed not in inactive gas but in atmosphere which contains reducing gas such as hydrogen fluoride (HF) at least in that case. Since sputter

etching advances returning a natural oxidation film of the surface of a vamp formed at a wetback's process by this by originating in oxygen and moisture which are incorporated into a vamp the surface of a vamp can be cleaned more effectively than the 1st invention.

[0023] Thus contact resistance with a probe or a printed-circuit board can be further reduced by the surface of a vamp after a result being defecated more effectively. As a result while the electrical property of a device which produced a vamp is improved substantially reliability and endurance of a product assembled by carrying out flip chip mounting of this device can be raised more than the 1st invention.

[0024] According to the 3rd invention in this invention two steps of plasma treatment are performed to a base after bump formation. Plasma treatment is performed in oxygen gas atmosphere it is the process reason of a wetback process or a resist process and specifically ashing removal of the impurity of an organic system adhering to the vamp surface is carried out by a combustion reaction ($C+O^{\circ} \rightarrow CO^{**}$). Then plasma treatment is performed in an inert gas atmosphere or a reducing gas atmosphere and sputter etching for defecating the vamp surface is performed like the 1st or 2nd invention. Thereby since impurity removal of an organic system can be performed effectively in addition to natural oxidation film removal on the surface of a vamp defecation on the surface of a vamp can be put into practice more than the 1st and 2nd inventions.

[0025] As a result like the 1st and 2nd inventions reduction of contact resistance of a vamp can be aimed at and high-reliability and high durability can be acquired now in a product assembled by carrying out flip chip mounting.

[0026]

[Embodiment of the Invention] Hereafter it explains referring to drawings for the embodiment of this invention. In the complete diagram of an embodiment the same numerals are given to the portion which is the same or corresponds.

[0027] First the manufacturing method of the solder ball bump by a 1st embodiment of this invention is explained. Drawing 1 is a sectional view for explaining the manufacturing method of the solder ball bump by this 1st embodiment.

[0028] That is in the manufacturing method of this solder ball bump first as shown in drawing 1 A sputtering process the RIE method etc. are used for the prescribed position on the semiconductor base substance 1 like the Si wafer in which the circuit element was formed and Al electrode pad 2 of specified shape is formed in it. Next an opening is formed in the portion corresponding to the Al electrode pad 2 top of this passivation

film after forming a passivation film (not shown) like an SiN film all over this semiconductor base substance 1. Next an opening is formed in the portion corresponding to the Al electrode pad 2 top of this polyimide film 3 after forming the polyimide film 3 in the whole surface. This polyimide film 3 has a role of the soft error prevention by a surface protection electric insulation and alpha rays.

[0029] Next by patterning mostly this Cr/Cu/Au membrane after identical shape with Al electrode pad 2 after laminating a Cr film a Cu film and Au membrane on the whole surface one by one for example and forming Cr/Cu/Au membrane in it by sputtering process BLM film 4 which consists of this patterned Cr/Cu/Au membrane is formed. This BLM film 4 also has a role of a barrier metal of the solder ball bump formed behind.

[0030] Next as shown in drawing 1 B After forming a resist film in the whole surface this resist film is patterned after specified shape by the lithography method. The numerals 5 show the resist pattern of the specified shape formed by this. This resist pattern 5 has the opening 6 of a predetermined size into the portion corresponding to the BLM film 4 top therefore the portion corresponding to the Al electrode pad 2 top.

[0031] Next as shown in drawing 1 C the solder film 7 is formed with a vacuum deposition method all over the semiconductor base substance 1. Next as shown in drawing 1 D a lift off removes the resist pattern 5 with the solder film 7 on it. Thereby the solder film 7 is patterned after desired shape. Next the flux (not shown) which uses pitch such as an amine system active agent an alcohol solvent rosin and polyglycol as the main ingredients is uniformly coated all over the semiconductor base substance 1 for example. Then by heat-treating using melting and surface tension of the solder film 7 as shown in drawing 1 E the almost spherical solder ball bump 8 is formed.

[0032] Then organic chemical washing is performed to the semiconductor base substance 1 and flux is removed. The numerals 9 show the impurity layer which consists of a contaminant resulting from the natural oxidation film formed in the surface of the solder ball bump 8 or a process etc. among drawing 1 E. Here the impurity layer 9 of the surface of the expedient top of expression and the solder ball bump 8 was exaggerated and it has written thickly.

[0033] In the manufacturing method of this solder ball bump as shown in drawing 1 F after performing even formation of the solder ball bump 8 by a wet back sputter etching processing is performed to the semiconductor base substance 1. Here the case where sputter etching processing is performed as an example using a parallel plate type high frequency plasma processor as shown in drawing 2 is explained. That is as shown in

drawing 2this parallel plate type high frequency plasma processor has the plasma treating chamber 11the positive plate 12and the cathode plate stage 13. The positive plate 12 is grounded and the cathode plate stage 13 is connected with the plasma power source 15 for plasma discharge via the coupling capacitor 14. As this plasma power source 15an RF generator with a frequency of 13.56 MHz is usedfor example. The numerals 16 show the processed board installed on the cathode plate stage 13.

[0034]In this parallel plate type high frequency plasma processorBy introducing process gas and supplying a predetermined plasma discharge output in the plasma treating chamber 11It is possible to perform sputter etching processing of the processed board 16 which made generate the plasma 17 between the positive plate 12 and the cathode plate stage 13and was installed on the cathode plate stage 13 by the ion irradiation from this plasma 17.

[0035]In the manufacturing method of the solder ball bump by this 1st embodiment. After forming the solder ball bump 8 with the semiconductor base substance 1 of the state which shows in drawing 1 Ei.e.a wetbackThe semiconductor base substance 1 in the state where the impurity layer 9 has adhered to the surface of the solder ball bump 8 is introduced into the parallel plate type high frequency plasma processor shown in drawing 2and sputter etching processing is performed in inert gas atmospheressuch as Ar gas.

[0036]Specificallysputter etching processing is performed on the following conditions as an example. That is25sccm and a pressure shall be 1.0 Pastage temperature is made into a room temperature for the flowa plasma discharge output is set to 300W (13.56 MHz)sputter etching processing is performedusing Ar gas as process gasand the processing time is carried out for 60 seconds.

[0037]As shown in drawing 1 Fas a result of this etching process by the sputtering action of Ar⁺ ion. While the impurity layer 9 formed in the surface of the solder ball bump 8 is removed effectively and the surface of the pure solder ball bump 8 is exposedthe surface of the polyimide film 3 which is a surface-protection film is chemically activated in response to ion bombardment energy.

[0038]Drawing 3 shows the example which carried out flip chip mounting of the LSI chip which performed above-mentioned sputter etching processing to the printed-circuit board after formation of the solder ball bump 8. In drawing 3the numerals 20 show the passivation film which consists of an SiN film formed on the semiconductor base substance 1. In this casean LSI chip is mounted in a printed-circuit boardas the solder ball bump 8 turns to the bottom. A printed-circuit board consists of the

glass epoxy board 2 and the Cu land 22 and the solder resist 23 on this. Where an LSI chip is mounted on a printed-circuit board alignment of an LSI chip and the printed-circuit board is carried out so that the position corresponding to the solder ball bump 8 may serve as the Cu land 22. These solder ball bumps 8 and the Cu land 22 of each other are connected by the eutectic crystal solder 24. The numerals 25 show the sealing resin which adheres an LSI chip on a printed-circuit board. [0039] According to this 1st embodiment by performing sputter etching processing to the semiconductor base substance 1 after formation of the solder ball bump 8 while the impurity layers 9 such as a natural oxidation film of the surface of the solder ball bump 8 are removed effectively and the surface of the pure solder ball bump 8 is exposed the surface of the polyimide film 3 which is a protective film is activated. By this while being able to measure now the electrical property of the solder ball bump 8 correctly the product assembled by carrying out flip chip mounting to a printed-circuit board as this device was shown in drawing 3 Since both the adhesion strength in the electrical property in the interface of the solder ball bump 8 and the Cu land 22 and the interface of the polyimide film 3 and the sealing resin 25 improve the reliability and endurance of a final product are substantially improved compared with the conventional thing.

[0040] Next a 2nd embodiment of this invention is described. The manufacturing method of the solder ball bump by this 2nd embodiment is the same as that of a 1st embodiment except performing sputter etching processing after solder ball bump formation using the triode type high frequency plasma processor shown in drawing 4.

[0041] Here the triode type high frequency plasma processor used in this 2nd embodiment is explained first. That is as shown in drawing 4 this triode type high frequency plasma processor has the plasma treatment apparatus 31 the positive plate 32 the lattice electrode 33 and the cathode plate stage 34. The positive plate 32 is connected with the plasma power source 36 for plasma production via the coupling capacitor 35 and the lattice electrode 33 is grounded. The cathode plate stage 34 is connected with the board bias power supply 38 for board bias via the coupling capacitor 37. As the plasma power source 36 an RF generator with a frequency of 2 MHz is used for example and an RF generator with a frequency of 13.56 MHz is used as the board bias power supply 38 for example. A plasma discharge output and substrate bias voltage are independently controlled by these plasma power sources 36 and the board bias power supply 38. The numerals 39 show the processed board installed on the cathode plate stage 34.

[0042]In this triode type high frequency plasma processorIt is possible by introducing process gas and supplying a predetermined plasma discharge output in the plasma treating chamber 3lto generate the plasma 40 between the positive plate 32 and the lattice electrode 33and to perform sputter etching processing of the processed board 39 by the ion irradiation from this plasma 40.

[0043]In this 2nd embodimentas shown in drawing 1 Etthe semiconductor base substance 1 after a wetback performs even formation of the solder ball bump 8Sputter etching processing is performed in the atmosphere containing reducing gasintroducing into an above-mentioned triode type high frequency plasma processor as a processed boardand controlling a plasma discharge output and substrate bias voltage independently.

[0044]Specificallysputter etching processing is performed on the conditions shown below as an example. The flow of HF gasusing the mixed gas of HF and Ar as process gas Namely10sccm20sccm and a pressure shall be 1.0 Pastage temperature is made into a room temperature for the flow of Ar gasa plasma discharge output is set to 700W (2 MHz)substrate bias voltage is set to 350V (13.56 MHz)sputter etching processing is performedand the processing time is carried out for 60 seconds.

[0045]According to this 2nd embodimentto the sputtering action of Ar⁺ ion in the case of sputter etching processing by in additionthe reducing action by HF. Since the impurity layers 9such as a natural oxidation film of the surface of the solder ball bump 8are removed much more effectivelybeing accompanied by a chemical reactionthe surface of the purer solder ball bump 8 is exposed. The dangling bond of the surface layer of the polyimide film 3 is terminated with a fluoride (F) atom with large electronegativityand will be in a chemical more activity state.

[0046]The product (refer to drawing 3) assembled by carrying out PURIPPU chip mounting of the LSI chip which performed sputter etching processing after solder ball bump formation as mentioned above on a printed-circuit boardThe adhesion strength in the electrical property in the interface of the solder ball bump 8 and the Cu land 22 and the interface of the polyimide film 3 and the sealing resin 25 improves furtherand the final reliability and endurance of a product are substantially improved like the case of a 1st embodiment compared with the former.

[0047]Nexta 3rd embodiment of this invention is described. The manufacturing method of the solder ball bump by this 3rd embodiment is the same as that of a 1st embodiment except performing ashing treatment and sputter etching processing after solder ball bump formation using the ICP high-density-plasma processing unit shown in drawing 5.

[0048] Here the ICP high-density-plasma processing unit used in this 3rd embodiment is explained first. That is as shown in drawing 5 this ICP high-density-plasma processing unit has the plasma treating chamber 41, the inductive coupling coil 42 and the stage 43. The joint induction coil 42 is connected with the ICP power supply 44 for plasma discharge and the stage 43 is connected with the board bias power supply 46 for board bias via the coupling capacitor 45. As the ICP power supply 44 an RF generator with a frequency of 450 kHz is used and an RF generator with a frequency of 13.56 MHz is used as the board bias power supply 46. A plasma discharge output (ICP source mode output) and substrate bias voltage are independently controlled by these ICP power supplies 44 and the board bias power supply 46. The numerals 47 show the processed board installed on the stage 43. Here the stage 43 is perpendicularly (direction shown by an arrow among drawing 5) movable.

[0049] In this ICP high-density-plasma processing unit it is possible by introducing process gas and supplying a predetermined ICP source mode output in the plasma treating chamber 41 to perform plasma treatment by the plasma 48 as for which more than $1 \times 10^{11} \text{cm}^{-3}$ has the density of less than $1 \times 10^{14} \text{cm}^{-3}$ for example.

[0050] In this 3rd embodiment as shown in drawing 1 the semiconductor base substance 1 after a wetback performs even formation of the solder ball bump 8. After performing ashing treatment in the atmosphere containing oxygen, introducing into an above-mentioned ICP high-density-plasma processing unit as a processed board and controlling independently an ICP source mode output and substrate bias voltages, sputter etching processing is continuously performed in the atmosphere containing reducing gas.

[0051] Specifically, ashing treatment is first performed on the conditions shown below as an example. The flow of O_2 using oxygen (O_2) as process gas, namely 100 sccm, a pressure shall be 1.0 Pa, stage temperature is made into a room temperature, ICP source power is set to 1000W (450 kHz), substrate bias voltage is set to 0V (13.56 MHz), ashing treatment is performed and the processing time is made into 10 seconds.

[0052] Next, conditions are switched as follows as an example and sputter etching processing is performed. The flow of HF gas using the mixed gas of HF and Ar as process gas, namely 10 sccm/20 sccm, and a pressure shall be 0.2 Pa, stage temperature is made into a room temperature for the flow of Ar gas, ICP source power is set to 1000W (450 kHz), substrate bias voltage is set to 100V (13.56 MHz), sputter etching processing is performed and the processing time is made into 10 seconds.

[0053] According to this 3rd embodiment, the surface layer of the polyimide

film 3 which is a protective film of a device serves as the form where O atom was incorporated during that combination by it at the same time the impurity of an organic system which adhered to the surface according to a process reason is effectively removed by ashing treatment by a combustion reaction.

[0054] And while the impurity layers 9 such as a natural oxidation film of the surface of the solder ball bump 8 are accompanied by a chemical reaction by the reducing action by HF, weld slag removal is effectively carried out by the sputter etching processing performed succeeding this and the surface of the purer solder ball bump 8 is exposed by it. The outermost superficial layer of the polyimide film 3 is terminated by F atom (it contains also when O atom introduced at the time of ashing treatment is replaced by F atom) and will be in a chemical still activity state.

[0055] The product (refer to drawing 3) assembled by carrying out PURIPPU chip mounting of the LSI chip which performed sputter etching processing after solder ball bump formation as mentioned above on a printed-circuit board. The adhesion strength in the electrical property in the interface of the solder ball bump 8 and the Cu land 22 and the interface of the polyimide film 3 and the sealing resin 25 improves further and the final reliability and endurance of a product are substantially improved like the case of 1st and 2nd embodiments compared with the former.

[0056] When performing the ashing treatment and sputter etching processing which are performed after formation of the solder ball bump 8 according to this 3rd embodiment using an ICP plasma source on high-density plasma and a concrete target. For example with more than $1 \times 10^{11} \text{cm}^{-3}$ processing with the plasma density of less than $1 \times 10^{14} \text{cm}^{-3}$ by this. It comes to enter into the semiconductor base substance 1 vertically without scattering about the ionic species generated so much when the processing under low-pressure power atmosphere was attained. For this reason the surface treatment (ashing treatment and sputter etching processing) of the semiconductor base substance 1 after the bump formation by ion irradiation -- a high speed -- and it is efficiently realizable.

[0057] Since it is possible to control independently the ion energy which enters into the semiconductor base substance 1 from plasma without affecting the creation state of plasma, shortening of processing time can be aimed at also on the conditions which set up substrate bias voltage low in consideration of the process damage to a device without causing the fall of processing speed.

[0058] Although the embodiment of this invention was described concretely

above this invention is not limited to an above-mentioned embodiment and it cannot be overemphasized that it is selectable suitably in the range which does not deviate from the main point of an invention such as sample structure, a process unit and a process condition.

[0059] For example, although the above-mentioned 1st - 3rd embodiment showed the case where the lift off of membrane formation by vacuum deposition and a resist pattern was used as a pattern formation method of a solder ball bump, application to the manufacturing method using the other electrolytic plating etc. is also possible.

[0060] Although 2nd and 3rd embodiments showed the example which used HF as gas of reduction nature, hydrogen (H_2) chloride (HCl) etc. can also be similarly used in addition to it. Among these, when using liquid source such as HF and HCl, it introduces in a process chamber with techniques such as bubbling by carrier gas such as helium (helium) heating evaporation and ultrasonic evaporation.

[0061]

[Effect of the Invention] As explained above, according to this invention, the natural oxidation film and process residue which were formed on the surface of the bump can be removed effectively and the surface of a pure bump can be exposed. As a result, the electrical property of the device which produced the bump improves -- having (contact resistance decreases) -- the reliability and endurance of the product assembled by carrying out PURIPPU chip mounting can be substantially raised now compared with the former.

[0062] Therefore, this invention is very effective in manufacture of the semiconductor device of which it is designed based on a detailed design rule and the degree of high integration, high performance and high-reliability are required.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]

[Drawing 1] It is a sectional view for explaining the manufacturing method of the solder ball bump by a 1st embodiment of this invention.

[Drawing 2] It is an approximate line figure showing an example of the parallel plate type high frequency plasma processor used in the manufacturing method of the solder ball bump by a 1st embodiment of this invention.

[Drawing 3] It is an approximate line figure showing the example which carried out flip chip mounting of the LSI chip which performed sputter

etching processing after solder ball bump formation to the printed-circuit board.

[Drawing 4] It is an approximate line figure showing an example of the triode type high frequency plasma processor used in the manufacturing method of the solder ball bump by a 2nd embodiment of this invention.

[Drawing 5] It is an approximate line figure showing an example of the ICP high-density-plasma processing unit used in the manufacturing method of the solder ball bump by a 3rd embodiment of this invention.

[Drawing 6] It is a sectional view for explaining the manufacturing method of the conventional solder ball bump.

[Drawing 7] It is an approximate line figure for explaining the situation of measurement of the electrical property of a solder ball bump.

[Description of Notations]

1 [... A BLM film5 / ... A resist pattern6 / ... An opening7 / ... A solder film8 / ... A solder ball bump9 / ... An impurity layer22 / ... Cu land25 / ... Sealing resin] ... A semiconductor base substance2 ... An Al electrode pad3 ... A polyimide film4
